AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1 - 3. (Canceled)

4. (Currently Amended) A fault analysis method for presuming a fault location of a semiconductor IC comprising:

applying a power supply voltage to said semiconductor IC;

supplying a test pattern sequence having a plurality of test patterns to said semiconductor IC;

storing ~~an analysis point included~~a fault location list for the test pattern sequence, wherein the fault location list includes one or more locations of components in said IC, and the electric potentials at the one or more locations are expected to~~of which~~ change[[s]] when the test pattern sequence is supplied~~in accordance with change of said supplied test pattern, to be corresponding to said test pattern sequence~~;

measuring a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern and determining whether said transient current shows abnormality or not; and

presuming a fault location out of said fault location list,~~analysis points~~ based on said test pattern sequence, where the transient power supply current shows abnormality, and said fault location list~~analysis point stored to be corresponding to said test pattern sequence~~,

wherein said transient power supply current is determined to be abnormal in case time integral of said transient power supply current is over a predetermined value in said step of determining.

5 - 15. (Canceled)

16. (Currently Amended) A fault analysis apparatus for presuming a fault location of a semiconductor IC comprising:

a means for applying a power supply voltage to said semiconductor IC;

a means for supplying a test pattern sequence having a plurality of test patterns to said semiconductor IC;

a means for storing ~~an analysis point included~~a fault location list for the test pattern sequence, wherein the fault location list includes one or more locations of components in said IC, and the electric potentials at the one or more locations are expected to ~~of which~~ change[[s]] when the test pattern sequence is supplied~~in accordance with change of said supplied test pattern, to be corresponding to said test pattern sequence~~;

a transient power supply current tester for measuring a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern and determining whether said transient current shows abnormality or not; and

a fault location presuming unit for presuming a fault location out of said fault location list, ~~analysis points~~ based on said test pattern sequence, where the transient power supply current shows abnormality, and said fault location list~~analysis point stored to be corresponding to said test pattern sequence~~,

wherein said transient power supply current tester determines that said transient power supply current is abnormal in case time integral of said transient power supply current is over a predetermined value.

17 - 26. (Canceled)

27. (Currently Amended) A fault analysis apparatus for presuming a fault location of semiconductor IC comprising:

a means for applying a power supply voltage to said semiconductor IC;

a means for supplying a test pattern sequence comprising a plurality of test patterns to said semiconductor IC;

a means for storing ~~an analysis point included~~a fault location list for the test pattern sequence, wherein the fault location list includes one or more locations of components in said IC, and the electric potentials at the one or more locations are expected to~~of which~~ change[[s]] when the test pattern sequence is supplied~~in~~

~~accordance with change of said supplied test pattern, to be corresponding to said test pattern sequence~~;

a means for measuring a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern;

a means for determining that said transient current is abnormal in case time integral of said transient power supply current is over a predetermined value; and

a means for presuming a fault location out of said fault location list,~~analysis points~~ based on said test pattern sequence, where the transient power supply current shows abnormality, and said fault location list~~analysis point stored to be corresponding to said test pattern sequence~~.